In the Claims:

1. (Currently Amended) A field-effect transistor with local source-drain insulation, having

a semiconductor substrate ~~(1)~~;

a source depression ~~(SV)~~ and a drain depression ~~(DV)~~, which are formed in a manner spaced apart from one another in the semiconductor substrate ~~(1)~~;

a depression insulation layer ~~(VI)~~, which is formed at least in a bottom region of the source depression ~~(SV)~~ and of the drain depression ~~(DV)~~;

an electrically conductive filling layer ~~(F)~~, which is formed for realizing source and drain regions ~~(S, D)~~ and for filling the source and drain depressions ~~(SV, DV)~~ at ~~the~~ a surface of the depression insulation layer ~~(VI)~~;

a gate dielectric ~~(3)~~, which is formed at ~~the~~ a substrate surface ~~(SO)~~ between the source and drain depressions ~~(SV, DV)~~; and

a gate layer ~~(4)~~, which is formed at ~~the~~ a surface of the gate dielectric ~~(3)~~,

wherein the source and drain depressions have, in an upper region, a widening with a predetermined depth for realizing defined channel connection regions.

2. (Currently Amended) The field-effect transistor as claimed in ~~patent~~ claim 1, wherein the depression insulation layer ~~(VI) furthermore~~ has a depression sidewall insulation layer ~~(8A)~~, which is formed in ~~the~~ a sidewall region of the source and drain depressions ~~(SV, DV)~~ but does not touch the gate dielectric ~~(3)~~.

3. (Cancelled)

4. (Currently Amended) The field-effect transistor as claimed in ~~one of patent claims 1 to 3~~ claim 1, wherein the electrically conductive filling layer ~~(F)~~ has a seed layer ~~(10)~~ for improving a deposition in the source and drain depressions ~~(SV, DV)~~.

5. (Currently Amended) The field-effect transistor as claimed in claim 1~~one of patent claims 1 to 4~~, wherein ~~the gate layer (4) has~~ a gate insulation layer ~~(6)~~ is formed at ~~its~~ sidewalls of the gate layer.

6. (Currently Amended) The field-effect transistor as claimed in claim 1~~one of patent claims 1 to 5~~, wherein ~~it~~ the field-effect transistor is bounded by shallow trench isolations ~~(2)~~.

7. (Currently Amended) The field-effect transistor as claimed in claim 1~~one of patent claims 1 to 6~~, wherein the field-effect transistor ~~it~~ has lateral structures < 100 nm.

8. (Currently Amended) The field-effect transistor as claimed in claim 1~~one of patent claims 1 to 7~~, wherein the source and drain depressions ~~(SV, DV)~~ have a depth ~~(d1+d2)~~ of approximately 50 nm to 300 nm.

9. (Currently Amended) The field-effect transistor as claimed in claim 2~~one of patent claims 2 to 8~~, wherein the depression sidewall insulation layer ~~(8A)~~ extends into a region below the gate dielectric ~~(3)~~.

10. (Currently Amended) A method for fabricating a field-effect transistor with local source/drain insulation, having the following steps:

a) ~~formation~~ forming and patterning ~~of~~ a gate stack with a gate layer ~~(4)~~ and a gate dielectric ~~(3)~~ on a semiconductor substrate ~~(1)~~;

b) forming ~~formation of~~ source and drain depressions ~~(SV, DV, V1, V2)~~ at the gate stack ~~(3, 4, 5, 6)~~ in the semiconductor substrate ~~(1)~~;

c) forming ~~formation of~~ a depression insulation layer ~~(8, 8A, 9)~~ at least in a bottom region of the source and drain depressions ~~(SV, DV)~~; and

d) filling ~~of~~ the at least partially insulated source and drain depressions ~~(SV, DV)~~ with a filling layer ~~(F; 10, 13)~~ for realizing source and drain regions ~~(S, D)~~

wherein, in step b), first depressions are formed for realizing channel connection regions in the semiconductor substrate, spacers are formed at the gate stack, and second depressions are formed using the

spacers as a mask in the first depressions and in the semiconductor substrate.

11. (Currently Amended) The method as claimed in ~~patent~~ claim 10, wherein, in step a),

an STI method is carried out for forming shallow trench isolations ~~(2)~~;

an implantation is carried out for forming at least one of well and/~~or~~ channel doping regions in the semiconductor substrate ~~(1)~~;

a thermal oxidation is carried out for forming the gate dielectric ~~(3)~~;

a deposition of semiconductor material is carried out for forming the gate layer ~~(4)~~;

a TEOS deposition is carried out for forming a hard mask layer ~~(5)~~;

a lithographic method is carried out for patterning at least the gate layer ~~(4)~~ using the hard mask layer ~~(5)~~, and

a further thermal oxidation is carried out for forming a gate sidewall insulation layer ~~(6)~~ at ~~the~~ sidewalls of the gate layer ~~(4)~~.

12. (Cancelled)

13. (Currently Amended) The method as claimed in ~~patent~~ claim ~~12~~10, wherein the first depressions ~~(V1)~~ are formed using the gate stack ~~(3, 4, 5, 6)~~ and the shallow trench isolation layer ~~(2)~~ as a mask down to a first depth ~~(d1)~~ of approximately 10 to 50 nm from the substrate surface ~~(SO)~~ by means of anisotropic etching.

14. (Currently Amended) The method as claimed in ~~patent~~ claim ~~12 or 13~~10, wherein, before the formation of the spacers ~~(7)~~, a first semiconductor protection layer is formed at least at the channel connection regions ~~(KA)~~.

15. (Currently Amended) The method as claimed in ~~one of patent claims 12 to 14~~claim 10, wherein the spacers ~~(7)~~ are formed by conformal deposition of silicon nitride and anisotropic etching-back.

16. (Currently Amended) The method as claimed in ~~one of patent claims 12 to 14~~claim 10, wherein the second depressions ~~(V2)~~ are formed down to a depth ~~(d1+d2)~~ of approximately 50 to 300 nm from the substrate surface ~~(SO)~~ by means of anisotropic etching.

17. (Currently Amended) The method as claimed in ~~one of patent claims 10 to 16~~claim 10, wherein, in step c),

an insulation mask layer ~~(8)~~ is formed in the source and drain depressions ~~(SV, DV)~~ and removed again at least in the bottom region; and

a depression bottom insulation layer ~~(9)~~ is in each case formed in the uncovered bottom region.

18. (Currently Amended) The method as claimed in ~~patent~~ claim 17, wherein, ~~furthermore,~~

the remaining insulation mask layer ~~(8)~~ is also removed at ~~the~~ sidewalls of the depressions; and

depression sidewall insulation layers ~~(8A)~~ are formed in the uncovered sidewall regions of the depressions.

19. (Currently Amended) The method as claimed in ~~patent~~ claim 17 ~~or 18~~, wherein

a silicon nitride layer is formed as insulation mask layer ~~(8)~~; and

a silicon dioxide layer is formed as at least one of a depression bottom and~~/or~~ sidewall insulation layer ~~(9, 8A)~~.

20. (Currently Amended) The method as claimed in ~~one of patent claims 10 to 19~~claim 10, wherein, in step d),

d1) a seed layer ~~(10)~~, a seed protection layer ~~(11)~~ and a seed mask layer ~~(12)~~ are formed over the whole area of the field-effect transistor;

d2) the seed mask layer ~~(12)~~ is caused to recede ~~right~~ into the source and drain depressions ~~(SV, DV)~~;

d3) the seed protection layer ~~(11)~~ is partially removed using the seed mask layer ~~(12)~~ as a mask;

d4) the seed mask layer ~~(12)~~ that was caused to recede is removed;

d5) the seed layer ~~(10)~~ is partially removed using the seed protection layer ~~(11)~~ as a mask;

d6) the seed protection layer ~~(11)~~ is completely removed; and

d7) a growth layer ~~(13)~~ is formed on the seed layer ~~(10) right~~ into a region of the substrate surface ~~(SO)~~.

21. (Currently Amended) The method as claimed in ~~patent claims 20 and 12~~claim 20, wherein,

in step d6), ~~furthermore,~~ the spacers ~~(7)~~ are removed; and

in step d),

d8) implantation spacers ~~(14)~~ are formed at the gate stack ~~(3, 4, 6)~~;

d9) the hard mask layer ~~(5)~~ is removed; and

d10) an implantation ~~(I)~~ is carried out for doping the gate layer ~~(4)~~ and also the growth layer ~~(13)~~.